Improved Parameter Extraction Procedure for PSP-Based MOS Varactor Model

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***Abstract*— We present an improved procedure for extracting parasitic capacitance parameters and gate current parameters for MOSVAR, the industry standard MOS varactor model. Our technique is verified against measured data from three technology nodes (180 nm, 130 nm and 65 nm), and is also used to validate the MOSVAR P-gate/P-well tunneling current sub-model.**

I. Introduction

For MOS varactor modeling, the Compact Model Council (CMC) has standardized the MOSVAR model model [1], which is based on the PSP MOSFET model model [2]. MOSVAR includes physical models for many phenomena, such as parasitic capacitances and resistances (cf. Fig. 1) and gate tunneling current. These effects are interdependent in real devices; for example, the combined overlap/fringing capacitance and the gate leakage current are correlated through overlap length and the effective channel length and width, which can make parameter extraction challenging [3]. (The overlap and fringing capacitances are lumped together in MOSVAR [1], and below we will use the term “fringing” capacitance to include both overlap and fringing capacitance).

In previous extraction procedures reported for MOSVAR [4] several simplifying restrictions were made, particularly as related to the fringing capacitances. The present work overcomes these restrictions by using a more elaborate analysis of experimental data. Our new method for MOS varactor parameter extraction enables simple determination of effective geometries, fringing capacitances, and the ratio of tunneling currents in overlap and channel regions. This leads to conclusive validation of the MOS varactor tunneling current sub-model [1].

In section II the new extraction methodology for effective geometries and fringing capacitances is introduced. Section III presents an improved procedure for channel and overlap gate current parameter extraction, based on the effective geometry determined in section II. Results from multiple technology nodes are presented. The conclusion follows in Section IV.

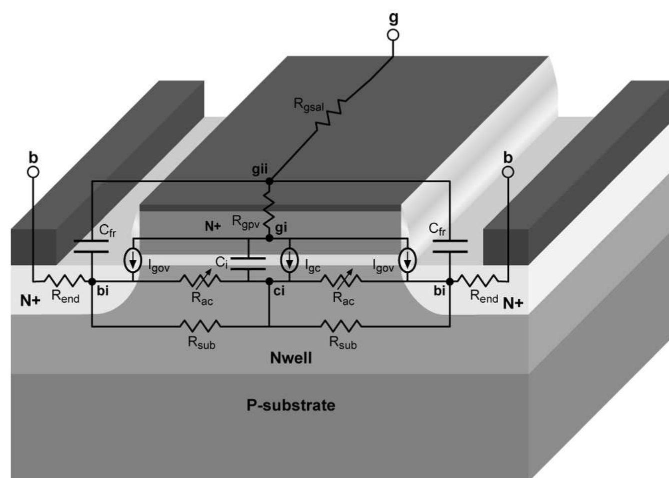

Fig. 1. N^+-poly/N-well MOS varactor with superimposed MOSVAR model network; after [1].

II. Fringing Capacitance and Effective Geometry Extraction

The MOS varactor capacitance defined in the MOSVAR model is given by

$$C(V) = C_o(V) \cdot L \cdot W \cdot m + C_{fr} \cdot m \quad (1)$$

where C_o is the bias-dependent capacitance of the intrinsic part of the device, the length and width are

$$L = L_g + \text{DLQ} \quad (2)$$

$$W = W_g + \text{DWQ} \ , \quad (3)$$

and m is the multiplicity factor. The combined fringing and overlap capacitance is given by

$$C_{fr} = 2 \cdot \text{CFRW} \cdot W + 2 \cdot \text{CFRL} \cdot L \ . \quad (4)$$

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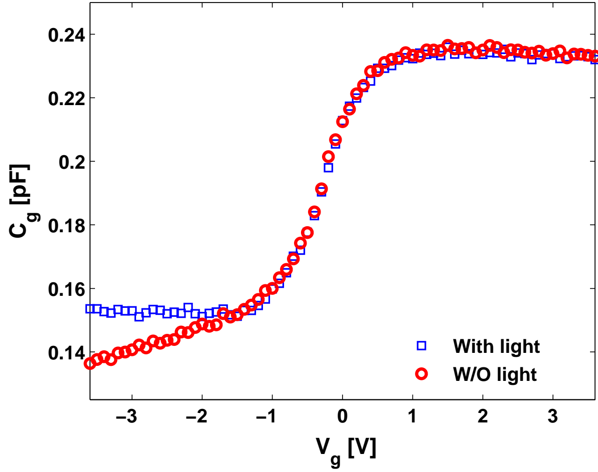
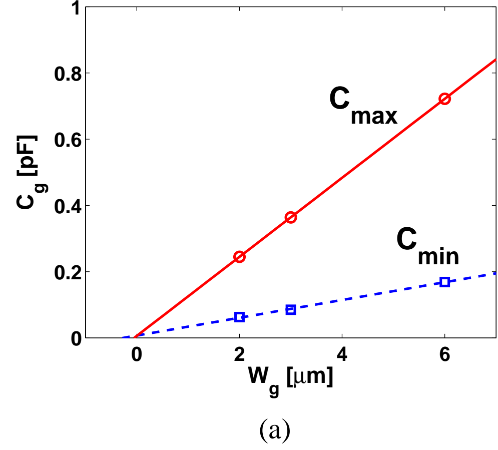


Fig. 2. Comparison of measured data between illuminated and dark measurement conditions.



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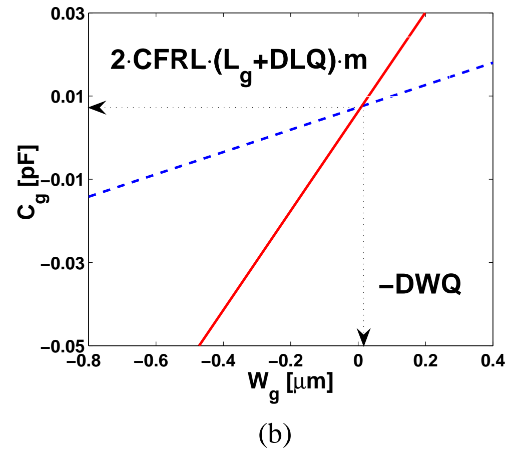


(b)

Fig. 3. (a) Measured $C_{min}(W_g)$ and $C_{max}(W_g)$ for a 180nm RFCMOS technology, $L_g = 0.5\ \mu m$, $m = 20$ and $f = 500$ MHz, and (b) Zoom-in of (a) near the intersection point.

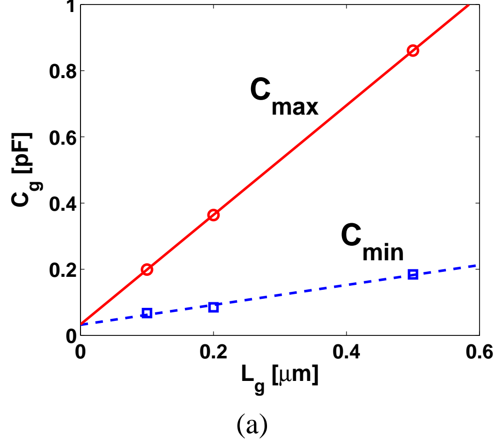
The parameters DWQ and DLQ represent the deviations of the effective channel length L and width W from their "design" or "drawn" values, L_g and W_g.

The parameter extraction task is to determine DWQ, DLQ, CFRW and CFRL from test data. In MOSVAR, CFRW encompasses the poly gate overlap of the well contact region (N^+ in the case of an N-well) and the fringing capacitance of the poly edge to silicon (as we have noted, a separate term for the overlap component is not included [1]). Previously, the parameters DWQ and DLQ were extracted assuming for simplicity that CFRL $= 0$ [4]. The CFRL term in the MOSVAR model encompasses capacitance associated with the poly gate extension onto STI and the fringing capacitances of the poly edges along the length. Neglecting CFRL presents difficulties in obtaining accurate $C(V)$ and $I_g(V)$ extractions over a wide range of device geometries. In this section we present a new parameter extraction procedure that does not assume that CFRL $= 0$.

Following [4], we consider the minimum and maximum values, C_{min} and C_{max}, respectively, of the high frequency capacitance C as determined from S-parameter measurements after de-embedding. To assure identical conditions for measurements and simulations special attention is paid to the frequency behavior of C in the inversion region, which directly influences the value of C_{min}. Fig. 2 shows typical $C(V)$ curves measured both with and without illumination. Without illumination the MOS varactor at least partially enters the deep depletion regime, which produces erratic values of C_{min} and complicates comparison with simulated results. Under illumination the time required for the inversion layer to form is reduced and a classical high-frequency MOS $C(V)$ curve is experimentally observed. The same $C(V)$ curve is simulated with the MOSVAR v1.0.0 model, which physically includes the frequency dependence of the inversion layer response to the applied voltage [5]. Thus illumination of the sample is required in order to produce consistent measurements of C_{min} for different devices.

Our extraction technique relies on linear regression fitting of C_{max} and C_{min} over geometry. From (1), formally $C_{min}(W_g) = C_{max}(W_g)$ when $W_g = -$DWQ. Hence at the intercept point of $C_{min}(W_g)$ and $C_{max}(W_g)$ for fixed L_g (as Fig. 3 shows) we have

$$XINT_{wg} = -\text{DWQ} \ , \tag{5}$$



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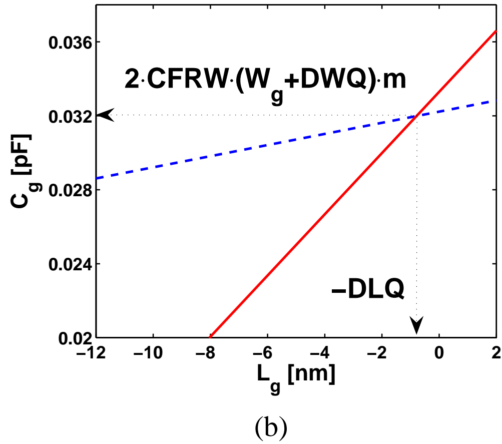


(b)

Fig. 4. (a) Measured $C_{min}(L_g)$ and $C_{max}(L_g)$ for a 180nm RFCMOS technology, $W_g = 3\ \mu m$, $m = 20$ and $f = 500$ MHz, and (b) Zoom-in of (a) near the intersection point.

$$YINT_{cwg} = 2 \cdot \mathrm{CFRL}(L_g + \mathrm{DLQ}) \cdot m\ . \qquad (6)$$

Similar linear extrapolation of $C_{min}(L_g)$ and $C_{max}(L_g)$ for fixed W_g, as Fig. 4 shows, yields

$$XINT_{lg} = -\mathrm{DLQ}\ , \qquad (7)$$

$$YINT_{clg} = 2 \cdot \mathrm{CFRW} \cdot (W_g + \mathrm{DWQ}) \cdot m\ . \qquad (8)$$

The parameters CFRL and CFRW are computed from (6) and (8), respectively, based on DLQ and DWQ from (7) and (5), respectively.

To verify this procedure, measured and modeled capacitances over bias for different device geometries, which have varying amounts of overlap and fringing capacitance, are shown in Fig. 5 for devices from a 180 nm technology, and in Figs. 6 and 7 for devices from a 130 nm technology. Capacitances over geometry for a 65 nm technology (not shown) are fitted equally as well.

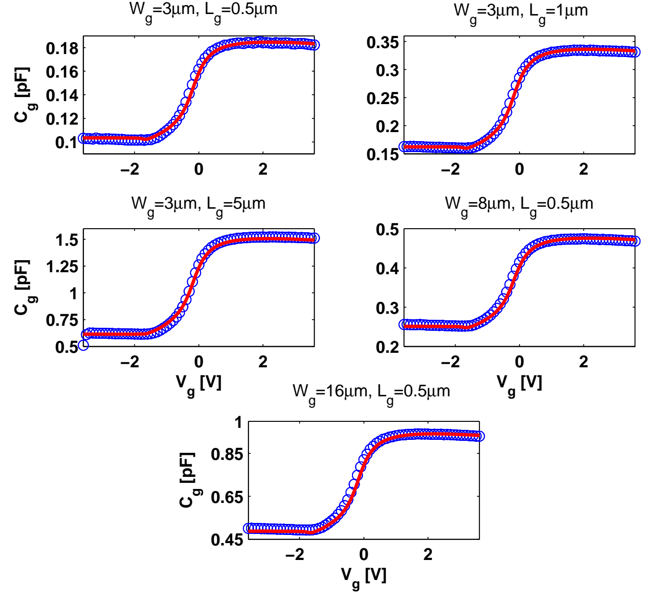


Fig. 5. Measured C(V) characteristics at $f = 500$ MHz (open circles) compared with simulation results (solid lines) for different device geometries in a 180 nm tecnology; $m = 20$.

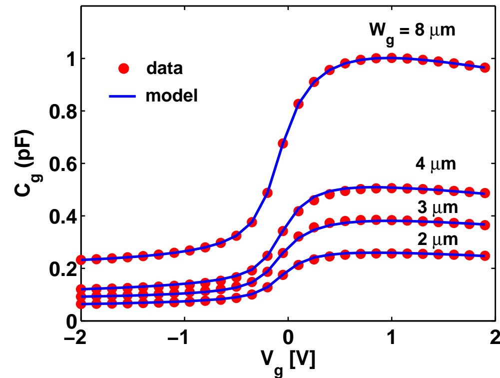


Fig. 6. Measured and simulated capacitances at $f = 1$ GHz for various W_g devices in a 130 nm technology; $L_g = 0.5\ \mu m$ and $m = 20$.

III. Gate Current Parameter Extraction and Model Verification

With DLQ and DWQ determined as described in section II, it becomes possible to find the relative magnitude of the gate tunneling current densities in the channel, i_{gc},

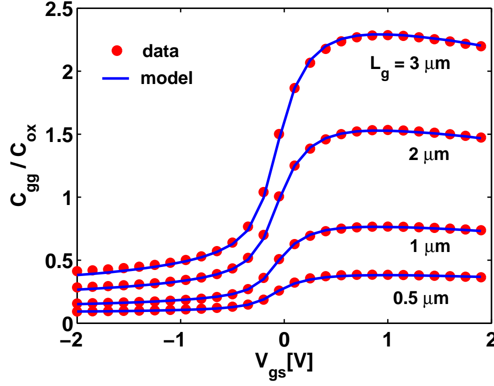


Fig. 7. Measured and simulated capacitances at $f = 1$ GHz for various L_g devices in a 130 nm technology; $W_g = 3$ μm and $m = 20$.

and in the overlap region, i_{gov}, contributing to the total gate current

$$I_g = I_{gc} + I_{gov} = i_{gc} \cdot L \cdot W \cdot m + i_{gov} \cdot W \cdot m \ . \quad (9)$$

This involves extracting the parameters IGCHVLW and IGOVHVW entering the expressions [1]

$$i_{gc}(V) = \text{IGCHVLW} \cdot D(V) \cdot F(V) \quad (10)$$

and

$$i_{gov}(V) = 2 \cdot \text{IGOVHVW} \cdot \text{LOV} \cdot D_{ov}(V) \cdot F_{ov}(V) \quad (11)$$

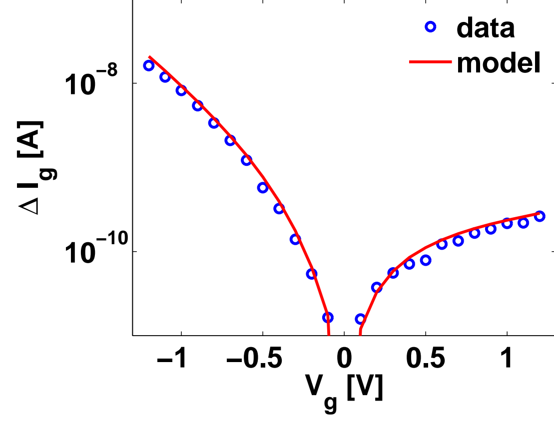
where $D(V)$ and $D_{ov}(V)$ are the tunneling transmission coefficients in channel and overlap regions, respectively, and $F(V)$ and $F_{ov}(V)$ are the associated supply functions [6]. The overlap length LOV $= 10$ nm used in this work was obtained from technology information.

To de-couple the gate current parameters for the channel region from those for the overlap region, $I_g(V)$ data from devices of maximum and minimum drawn channel length, L_{gmax} and L_{gmin}, are used. The difference in these currents is

$$\Delta I_g = \text{IGCHVLW} \cdot D(V) \cdot F(V) \cdot (L_{gmax} - L_{gmin}) \cdot W \cdot m \quad (12)$$

which does not depend on the gate current in the overlap region. The parameters IGCHVLW, GCOHVO, GC2HVO and GC3HVO, which model the gate-to-channel region tunneling current, are determined by fitting ΔI_g defined by (12) (see Fig. 8a).

The total gate current of the minimum length device has the greatest relative contribution from gate current in the overlap region, and so is what should be used



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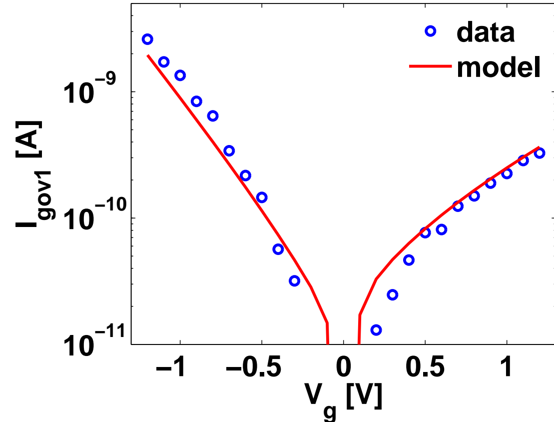

(b)

Fig. 8. (a) Measured and simulated $\Delta I_g(V)$ of (12) for $L_{gmax} = 0.5$ μm, $L_{gmin} = 0.1$ μm, and $W_g = 3$ μm, and (b) Measured and simulated $I_{gov1}(V)$ of (13) for $L_{gmin} = 0.1$ μm and $W_g = 3$ μm; devices used are in a 65nm RFCMOS technology.

to determine the parameters of the overlap region gate current model. At a given bias, the channel region gate current per unit length is given by $\Delta I_g/(L_{gmax} - L_{gmin})$, and this should be scaled by the effective length, see (2), to determine the intrinsic channel region current. This can then be subtracted from the total measured gate current of the minimum length device, $I_{g1}(V)$, to give the overlap region gate current

$$I_{gov1}(V) = I_{g1}(V) - \Delta I_g \cdot \frac{L_{gmin} + \text{DLQ}}{L_{gmax} - L_{gmin}} \ . \quad (13)$$

The parameters IGOVHVW and NOVO [1] can then be determined by fitting this current, see Fig. 8b.

The remaining parameters of the MOSVAR v1.0.0 model, including the parasitic resistances, are extracted as explained in [4].

Typical gate current fitting results are shown in Figs. 9 and 10 for a 130 nm CMOS process and in Figs. 11 and 12 for a 65 nm RFCMOS process. The good agreement between measurements and the model further validates our DLQ and DWQ extraction procedure presented in section II.

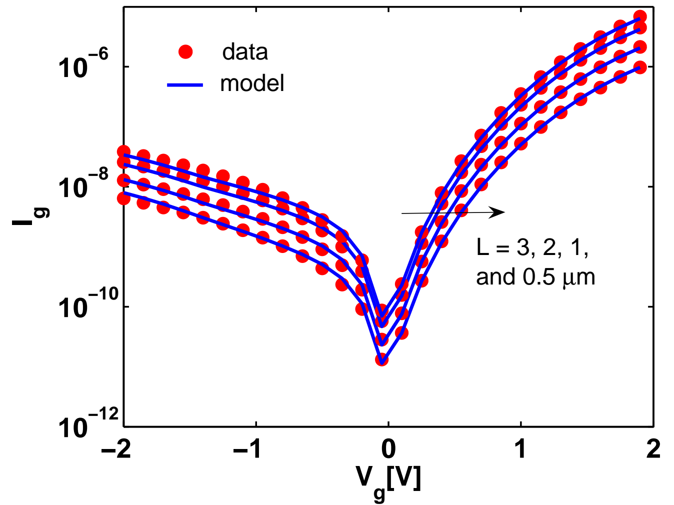

Fig. 9. Measured and simulated gate tunneling current for various W_g devices in a 130 nm technology; $L_g = 0.5\ \mu m$ and $m = 20$.

IV. Conclusion

We have presented a new procedure to determine parameters of the MOSVAR varactor model, and have verified the technique by fitting $C(V)$ and tunneling current measurements over multiple geometries for several technology nodes.

Acknowledgements

We would like to acknowledge I. Amano and R. Hiroyuki of Fujitsu Microelectronics Limited for providing the data for the devices in the 65nm technology node. This work was supported in part by the Compact Model Council.

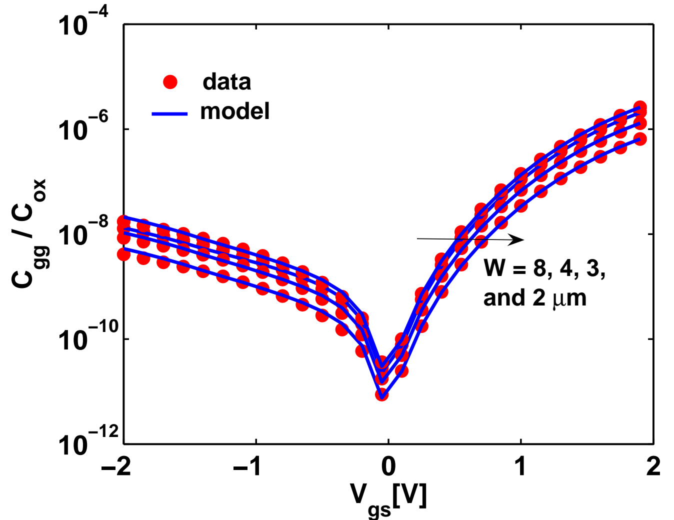

Fig. 10. Measured and simulated gate tunneling current for various L_g devices in a 130 nm technology; $W_g = 3\ \mu m$ and $m = 20$.

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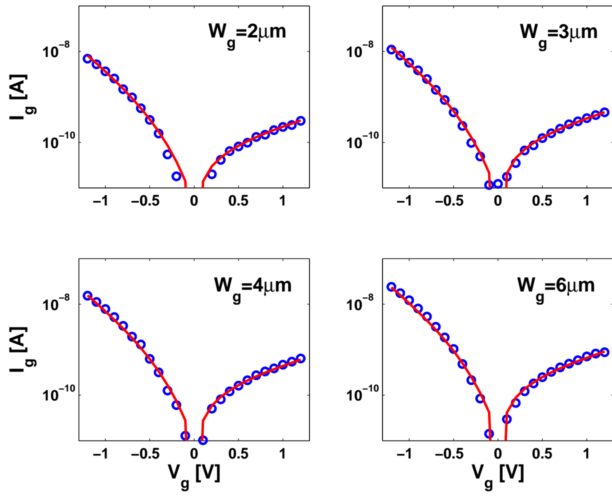

Fig. 11. Measured (oen circles) and simulated (solid line) gate tunneling current for various W_g devices in a 65nm RFCMOS technology; $L_g = 0.2$ μm and $m = 45$.

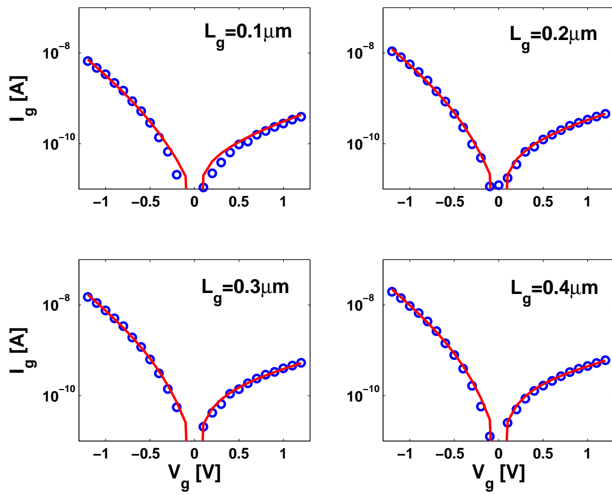

Fig. 12. Measured (open circles) and simulated (solid line) gate tunneling current for various L_g devices in a 65nm RFCMOS technology; $W_g = 3$ μm and $m = 45$.